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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/725,974	12/02/2003	Santosh Savkar	15148US02	4960
23446 7590 07/26/2007 MCANDREWS HELD & MALLOY, LTD 500 WEST MADISON STREET SUITE 3400 CHICAGO, IL 60661			EXAMINER TAYONG, HELENE E	
			ART UNIT 2611	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/725,974

Applicant(s)

SAVEKAR ET AL.

Examiner

Helene Tayong

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 02 December 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12/2/2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed on 5/507, have been fully considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-6, 11-12 and 13-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Kono et al (US 20010005398 A1).

(1) with regards to claims 1,13,15,16,18 and 19;

Kono et al teaches a method (Fig.6) for displaying images on a display comprising:

a decoder (52) for decoding encoded images and parameters associated with the images (pg.5, [0066], lines 3-5).

image buffers (58) for storing the decoded images pg. 5, [0066], lines 7-10) ;

parameter buffers (53) for storing the decoded parameters associated with the decoded images(pg. 5, [0067], lines 2-6) ; and

a display manager (55) for determining when to overwrite an existing image in the image buffers and providing a signal to the decoder indicating when to overwrite the existing image in the frame buffer(pg.6,[0075] and [0080]-[0081]); and

wherein the decoder overwrites the existing image after receiving the signal (pg.6, [0081], lines 4-7).

(2) with regards to claim 2;

The second reference further discloses wherein the set of parameters includes a parameter indicating when the system is utilizing a technique requiring selective images to be displayed more than once (pg. 6, [0086], lines 7-11).

(3) with regards to claim 3 ;

wherein the system for displaying images on a display further comprises:

a first processor (54);

a second processor (55);

a first memory (58);

a second memory(53); and

wherein the first memory stores an instruction set for the decoder (pg.6, [0079]).

(4) with regards to claim 4;

wherein the first processor (54) executes the instruction for the decoder(pg. 6, [0081] lines 3-4).

(5) with regards to claim 5;

wherein the second memory stores (53) an instruction set for the display manager (pg.6, [0085], lines 6-8), the instruction set for the display manager (fig.6, 68) executed by the second processor (pg.6, [0085], lines 8-11),.

(6) with regards to claim 6;

wherein the second processor (55) determines when to overwrite the existing image (pg. 6, [0084]-[0086]).

(7) with regards to claim 11;

the second memory stores the image buffers (fig. 6, 53d), (pg. 5, [0067]).

(8) with regards to claim 12;

wherein the second memory stores the parameter buffers (fig. 6, 53e), (pg. 6 [0067]).

(9) with regards to claim 13;

a first processor; and

a first memory connected to the processor (fig. 6, 51, the first memory storing instructions(pg.6, [0079]). wherein execution of the instructions by the first processor causes:

decoding images; and overwriting an existing image after the processor receives a signal indicating when to overwrite the existing image (pg. 5, [0080]).

(10) with regards to claim 14;

wherein execution of the instructions by the first processor further causes:
displaying the images(fig. 7 and fig.8).

(11) with regards to claim 15;

a second processor connected to the integrated circuit (fig. 6,55); and

a second memory connected to the processor (fig. 6, 53), the second memory storing instructions, wherein execution of the instructions by the second processor causes: determining when to overwrite the existing frame (pg. 5, [0080]); and

transmitting the signal to the first processor indicating when to overwrite the existing frame(pg. 5, [0081]).

(12) with regards to claim 16;

wherein execution of the instructions in the first memory by the first processor further causes: decoding parameters associated with the images (pg.6,[0080]).

(13) with regards to claim 17;
examining some of the decoded parameters associated with the images by the second processor (pg. 6, [0085], lines 10-11).

(14) with regards to claim 20;
determining when to overwrite the existing image (pg. 6, [0080]); and
transmitting a signal indicating when to overwrite the existing image (pg. 6, [0081], lines 4-7).

(15) with regards to claim 21;
decoding parameters associated with the images (pg. 6, [0080]);
and examining some of the decoded parameters associated with the images (pg. 6, [0085], lines 10-11);

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 7, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al (US 20010005398 A1) in view of Jiang et al (US 6614441).

(1) with regards to claims 7, 8 and 10;

Kono et al. discloses in (fig. 6) an integrated circuit comprises the first processor(53) and first memory (51).

Kono et al fails to teach wherein the second processor is off-chip from the integrated circuit.

However, Jiang et al in the same field of endeavor teaches wherein the second processor is off-chip from the integrated circuit as recited in claim 7 (col. 9, lines 44-47) and

The second reference further discloses where the second memory is an off-chip memory as recited in claim 8 (col. 9, lines 44-47)

The second reference further discloses where the second memory is DRAM as recited in claim 10 (col. 9, lines 44-47).

It would have been obvious to one of ordinary skill at the time of the invention to utilized the method of Jiang et al in the method of Kono et al in order to process video data in a computer system. The motivation to add Jiang's method in the method of Kono et al 's method would be to improve on display sequence management in a computer system.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kono et al in view of Xiang et al (US 20070153133 A1).

(1) with regards to claim 9;

Kono et al discloses all of the subject matter disclosed above but fails to teach wherein the first memory is a SRAM;

However, Xiang et al in the same field of endeavor teaches a SRAM (fig. 2, 204).

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It would have been obvious to one of ordinary skill at the time of the invention to utilized the memory of Xiang et al in the method of Kono et al in order to provide a video processing system having a processing unit. The motivation to add Xiang et al 's memory in the method of Kono et al would be to generate random burst addresses for processing of video signal.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Takabatake et al.(US 6320909 B1) discloses a memory having a storage capacity of storing pixel data of one frame.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helene E. Tayong whose telephone number is (571) 270-1675. The examiner can normally be reached on Monday - Friday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Liu Shuwang can be reached on (571) 272-3036. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Helene Tayong

7/23/07



SHUWANG LIU
SUPERVISORY PATENT EXAMINER